

DDR2 SDRAM SystemVerilog Verification IP

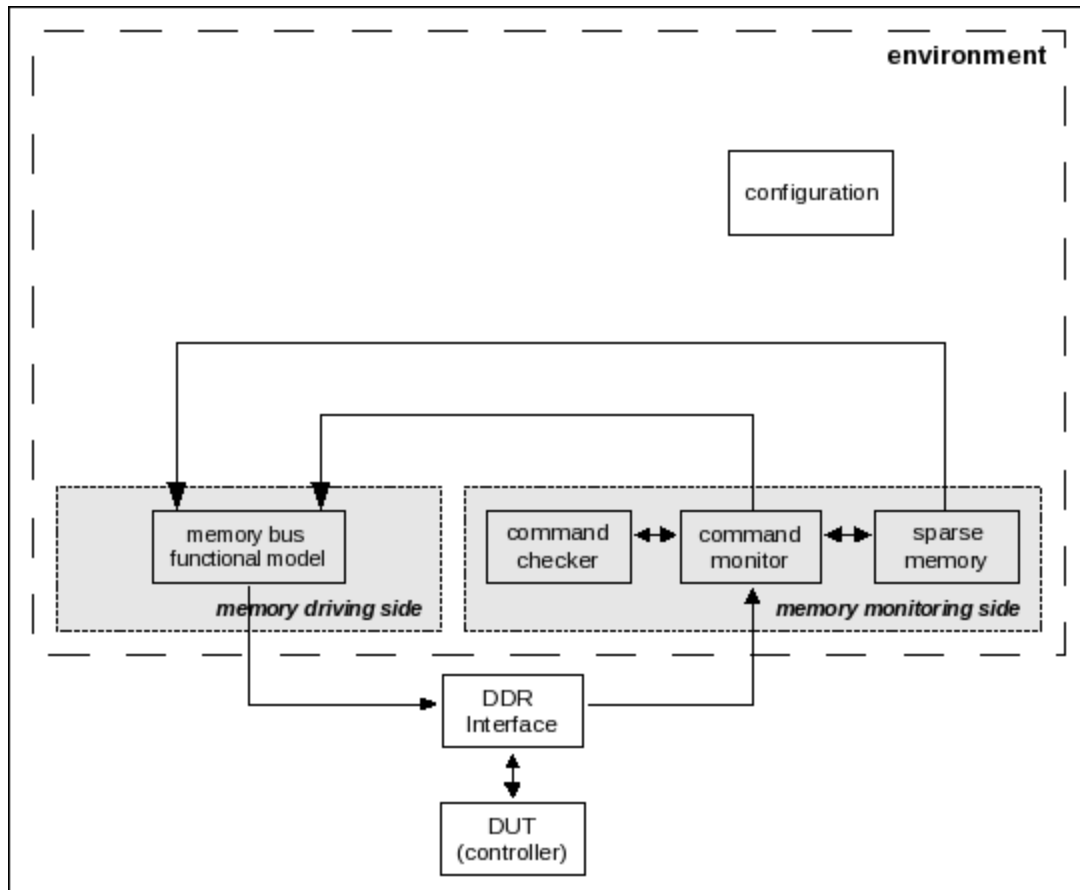
Overview

DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank/eight-bank DRAM. It uses a double-data-rate (DDR) architecture to achieve high speed operation.

NoBug DDR2 SDRAM SystemVerilog VIP comprises a complete set of elements for stimulating, checking and collecting coverage information of your device under test (DUT) implementation.

Features

- Compliant with JESD79-2E standard
- SystemVerilog VIP built on top of VMM (1.1.1)
- Implements both controller and memory functionalities
- Parameterizable number of stacks (ranks)
- Parameterizable number of banks
- Parameterizable data and data strobe bus width
- Configurable burst lengths
- Supports sequential and interleaved burst types
- Configurable CAS Latency and Additive Latency
- Configurable initialization procedure
- The default behavior of controller transactors implements Simplified State Diagram described by JESD79-2E standard, chapter 3.1
- User has a per-bank control of commands using commands sequences and commands sequences generators
- Rich set of callbacks
- Injection of erroneous cases (timing violations, illegal commands sequences)
- Assembly of collected data into structures using built-in monitors
- Functional coverage
- Protocol checkers (full timing checks, commands validity).



Example of verification environment architecture for verifying a controller

Deliverables

- Documentation (user guide, release notes)
- Encrypted SystemVerilog sources
- Example test cases
- Shell script for quick demo.

About NoBug

NoBug (www.nobug.ro) is an expert digital design verification company that masters a full range of technologies (functional, formal, assertion-based) with a variety of tools. Our goal is to establish strategic alliances designed to help deliver a customer-centric, total solutions approach to solving problems, exploiting business opportunities and creating sustainable competitive advantage for the customers.